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Test Services & Failure Analysis Laboratory

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Newsletter

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RESOURCES

CALCE TSFA Website

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The Reality of Flip-Chip Solder Bump Electromigration Failure

As flip-chip solder bump interconnects shrink to meet requirements for large numbers of I/O and small die size, the demand for the solder bump to carry high current density increases. It is possible that these solder bump interconnects could carry current densities on the order of 100 A/cm^2 in some applications. Although this current density is lower than that carried in device aluminum or copper interconnect lines, greater atomic diffusivity in the solder is expected because the solder has a much lower melting temperature than that of the device interconnects. Consequently, high current stress or electromigration related flip-chip failures are expected to increase. For further information, please contact Bhanu Sood (bpsood@calce.umd.edu).

Solder Joint Failure Criteria

The specification of a failure criterion for solder joints is an important element in the qualification of an electronic product. A common approach to reliability testing is to monitor electrical resistance during the testing. The techniques employed for resistance monitoring and data acquisition will determine whether information regarding transients or long-term drift is captured by the measurement. In order to obtain meaningful reliability data from tests, it is critical to choose a proper failure criterion and use the appropriate measurement technique to monitor the failure events. However, the definition of failure of a solder joint and its detection are neither straightforward nor standard. Failure criteria that require the periodic interruption of the test may significantly prolong the time required for the test, may miss a transient failure event, or may influence the results. On the other hand, continuous monitoring may capture a transient failure event but could produce false failures due to noise.

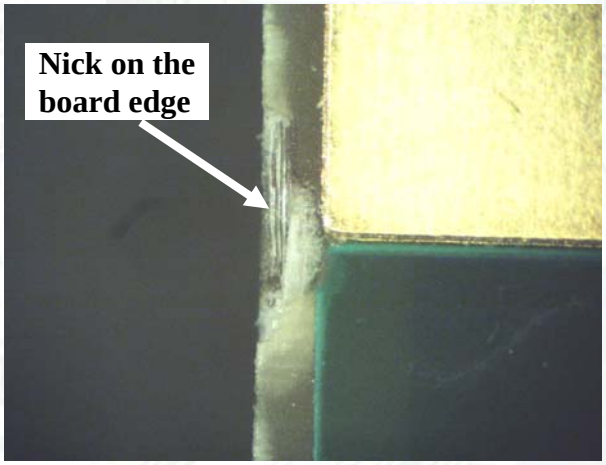
The failure criteria defined in the industry and professional standards differ. For example, there can be a 25 ohms or 300 ohms threshold, or a twenty percent increase from the baseline resistance. The times to failure for these three criteria can be significantly different. In one accelerated stress test of surface-mount test board vibration run by CALCE, these differences were as high as twenty percent of the time to failure. There is often no need to commit to failure criteria ahead of time; actually, it is best to gather the resistance information with time and stress conditions such as temperature, strain, and so on. The data can then be analyzed off-line to apply multiple failure criteria as appropriate from the application point of view. For details please refer to http://www.calce.umd.edu/articles/abstracts/2007/criteria.htm

External Inspection of PCBs

Applications with high input/output designs for specific integrated circuits are pushing printed circuit board (PCB) manufacturing technology to feature smaller sizes, higher layer counts, and more complex boards. Today, a typical multi-layered PCB has thousands of high aspect ratio plated-through holes, closely spaced line traces, and power/ground planes. Substantial concerns have arisen over the quality of PCBs, given the increasing density and complexity. Reductions in line spacing and via diameters and an increased number of vias and layers make the electronic products of today and tomorrow much more susceptible to defects introduced during the board fabrication process. Operating environments with extended temperature and humidity ranges can also increase a PCB's susceptibility to failures that are exacerbated by these defects. These design complexities call for a tighter process window during the PCB manufacturing process. Stringent PCB qualification measures are essential to assess board fabricator capabilities and the quality of finished unpopulated PCBs.

An upfront evaluation of PCB manufacturers based on their ability to meet reliability requirements can provide a valuable competitive advantage. A manufacturer's capability to design for reliability and to implement a reliable design through manufacturing and testing can yield important information about the likelihood that the company will provide a reliable product.

CALCE receives numerous requests for quality testing of PCBs. External inspection of a PCB is one aspect of quality testing. External inspection includes the board edges; base laminate; plated/non-plated holes; surface finish; screened, inked, or etched marking; solder resist registration; via hole tenting; flatness; and so on. It is performed as per IPC-A-600, IPC-6012, IPC4101, IPC-TM-650 and GR-78-CORE. Some common defects observed in PCBs by CALCE are nicks on the board edges, surface plating defects, blisters or wrinkles in the solder resist, nodules and burrs in plated-through holes, and filled through holes. For further information, please contact Bhanu Sood (bpsood@calce.umd.edu).



Hollow Fibers Continue to Cause Concern

In the March 2008 edition of the TSFA newsletter, we overviewed the origins of hollow glass fibers during manufacture. As a result of that article, CALCE has received various laminates in which to assess hollow fibers. In particular, CALCE received various Kingboard Chemical Holdings, Ltd PCB laminates for assessment of hollow fibers. Two Kingboard laminates, KB-6160 and KB-6167, had highly unacceptable hollow fiber concentrations. Other laminates that were tested included Shengyi S1170 and Shengyi S1155, and these samples had acceptable levels of hollow fibers. Hollow fibers can leave the printed circuit boards prone to CFF, which can lead to catastrophic failures.

Readers should know that some laminate companies, such as Nanya make their own resins, fibers (yarn), and weave their own fabric. Nanya is very aware of hollow fibers and makes concerted efforts to ensure that laminates are hollow filament free. Other companies, such as Isola (mentioned in the last TSFA newsletter) have some fabric weaving capability, but do not manufacture the fibers (yarns), where hollow fibers can be created. And other laminate suppliers do not manufacture either the fibers or weave the fabric. These companies must therefore carefully select their supply chains to obtain fabric from fiber (yarn) manufacturers that do not produce hollow fibers. In discussions between Prof Pecht and Isola CTO Tarun Amla, it is clear that Isola understands that the supply chain is complex and that they must continue to monitor the weavers and the fiber (yarn) manufacturers. In fact, Isola has data showing variation in the level of hollow filaments across fiber (yarn) producers, and continues to monitor and control their supply chain.

CALCE recommends that companies that purchase circuit boards, have a good understanding of the complete supply chain. If the manufacturers of circuit boards cannot tell you which company produces the fiber (yarn), such circuit boards should not be purchased. In addition, CALCE recommends that laminate samples are obtained from the circuit board manufacturer so that hollow fiber analysis can be conducted.

Printed circuit board laminates composed of hollow fibers continue to pose a threat to the reliability of electronic systems, in that they provide a convenient path for conductive filament formation (CFF). If a hollow fiber connects two conductors, metallic copper ions with moisture, can migrate from one conductor to the next, eventually forming a continuous bridge that constitutes an electrical leakage path or a short. The CALCE TSFA Laboratory continues to observe a significant number of PCB product failures due to hollow fibers. For further information, please contact Prof. Michael Pecht (pecht@calce.umd.edu).

Measurement of Tin Whisker Breakdown Voltage

Tin whisker is a conductive crystalline tin structure growing from the tin surface. It causes electrical shorts between adjacent leads of a component because it can grow to touch both surfaces. The whisker is covered with electrically insulating films, such as tin oxide, so mechanical contact does not cause a short circuit until a breakdown occurs in the tin oxide layer. To assess the breakdown of tin whisker oxide, CALCE set up an experimental circuit using a semiconductor parametric analyzer and a micromanipulator. Voltage ranging from 0 V to 50 V was applied to the whisker using a tungsten and gold probe, and the I-V relationship was simultaneously recorded. The force applied by the probe on the whisker was estimated by measuring the deflection of the whisker. The breakdown between the whisker and the tin-plated leadframe was examined using the experimental circuit.

Figure 1. Experimental setup for measuring the breakdown voltage

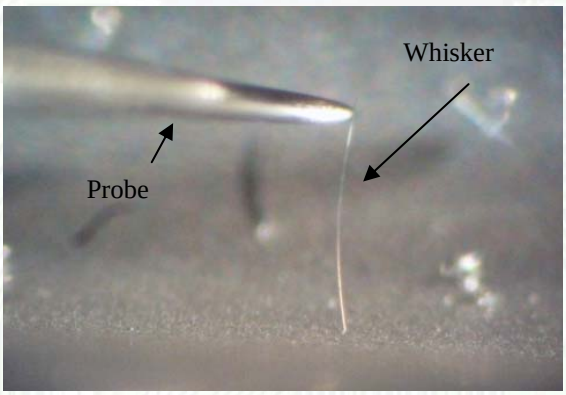


Figure 2. The whisker was bent by the mechanical contact of the probe

CALCE Provides 3-Step Part Authenticity Risk Assessment

CALCE provides inspection and testing services to verify the authenticity of electronic parts and identify the risk of parts being counterfeit. The philosophy behind our process is to identify parts with high risk of being counterfeit in a step by step manner so that a decision can be reached regarding possible problems with parts in lower cost and time.

We divide the tasks in three steps going from least intrusive and time consuming ones and progressing to more complicated and intrusive tests. The common evaluations at each such step are listed below. At the end of each step, the customer is provided with our risk assessment so decision can be made on whether further investigation to the next steps are necessary. The customer is also given report on possible quality and reliability risks of the parts in addition to authentication risks.

The cost of the evaluation will depend on the type and number of parts. Individual cost estimates are provided for each request. We will also work with the customers to determine the types of samples and documentation that will be necessary to perform the risk assessment. For further information, please contact Dr. Diganta Das (digudas@calce.umd.edu) or Bhanu Sood (bpsood@calce.umd.edu).

Step A

- Documents check (e.g., certificate of conformance, traceability, and test reports).
- Visual inspection (e.g., part markings, part termination quality, surface quality)
- Marking permanency tests (for ink marked parts)
- X-ray inspection (e.g., die size, interconnect alignment, internal assembly)

Step B

- X-ray fluorescence spectroscopy (to verify the elemental composition of part termination materials)
- Scanning acoustic microscopy (to detect popcorn cracking in molding compounds, and interfacial delamination) to detect possible part damage.
- Electrical tests (using curve tracer for active parts, LCR meter for passive parts), if necessary over a temperature range.

Step C

- Destructive tests
- Package decapsulation (to verify die markings, passivation layer quality, interconnect quality)
- ESEM/EDX analysis (to verify the elemental composition of a cross-section of the delidded part)
- Functional and parametric tests

Rework Limits with Lead-free Tin-Silver-Copper (SAC) Solders

Tin-Silver-Copper (SAC) solder, the leading replacement for tin-lead solder, is very aggressive in dissolving copper during reflow. The copper dissolution issue limits the number of reworks that may be attempted on printed wiring assemblies. In particular, solder fountain rework used in removing pin in hole packages can lead to complete removal of copper plating between the copper pad and the copper barrel. Recently, CALCE has evaluated rework of lead-free SAC BGA packages. In this study, the reduction in pad thickness has been identified and limiting factor with lead-free (SAC) BGA rework. In addition, CALCE has observed edge effects that may further reduce rework and due to potential trace damage. If you are interested in have CALCE assess your rework process, please contact Dr. Michael Osterman (osterman@calce.umd.edu).

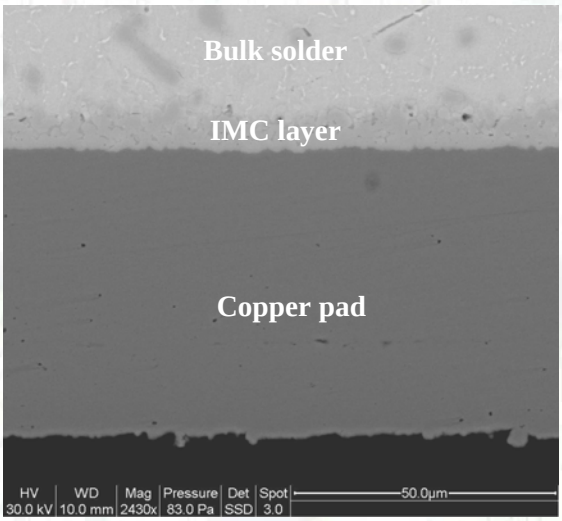


Figure1: Solder/pad interface in lead-free assemblies without rework

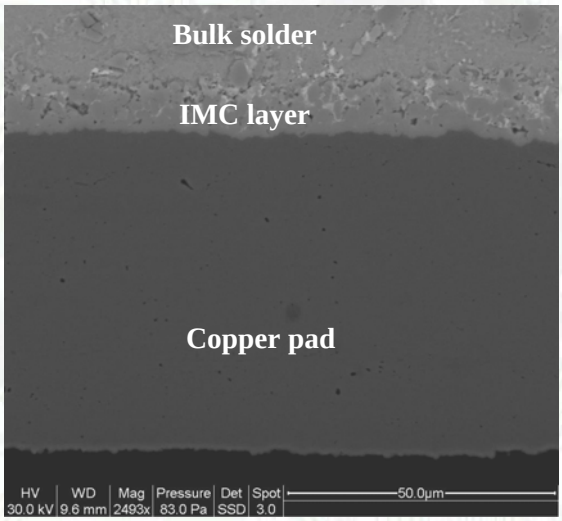


Figure 2 : Solder/pad interface in mixed assemblies without rework

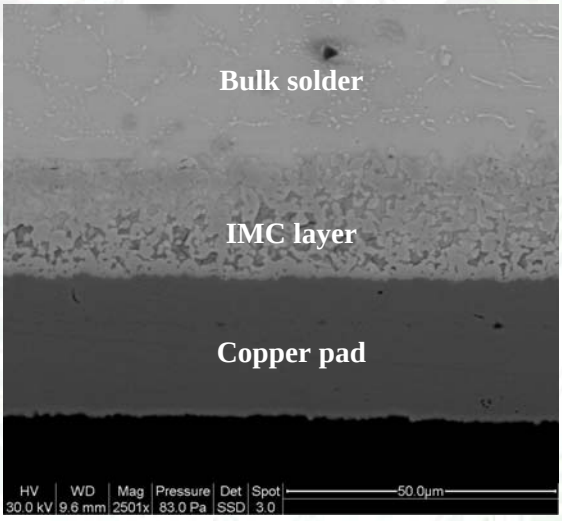


Figure 3:older/pad interface in lead-free assemblies after five replacements

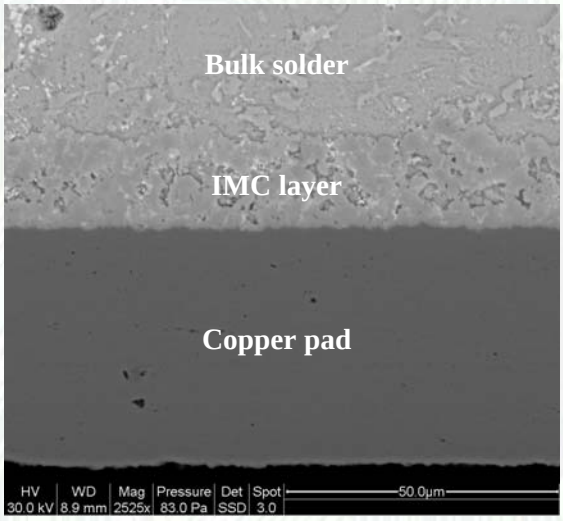


Figure 4: Solder/pad interface in mixed assemblies after five replacements